**RISC-V Class Project Phase 8 – MEMCTL Design**

This document provides an actual design for the MEMCTL function.

1. **Codasip Code**

Figure 1 Show a working version of the code for the ex\_memctl() block. This is a state machine with r\_me\_memcnt as the state register, r\_ex\_memop as the control input and some registers to save various values. Note that you will need to assert s\_ex\_stall if s\_ex\_resp indicates a WAIT.

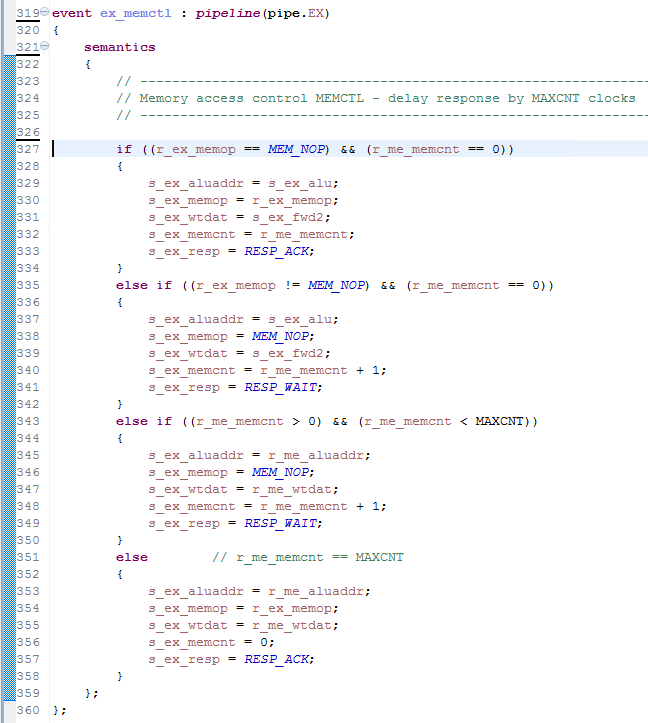


Figure 1

1. **Other Modifications**

Add any necessary signals and registers to the ca\_resources.codal file.

Note that some signals may have different names than in your design. Use your schematics to update the ex\_memctl() code.